Remarks

In the Office Action, the Examiner noted that claims 1-42 are pending in the application, and that claims 1-42 are rejected. By this amendment, claims 2, 12, 19-30, and 39-42 have been canceled; claims 43-70 have been added; and claims 1, 3, 4, 11, 13, 16, 31, 32, and 34 have been amended. Thus, claims 1, 3-11, 13-18, 31-38, and 43-70 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Oath/Declaration

Applicant notes the Examiner's indication that the declaration as originally submitted is defective because the title reflected in the declaration does not match the title in the specification. Applicant will submit a supplement declaration with the proper title on indication of allowable subject matter.

In the Specification

The Examiner objected to the specification. Applicant has amended the summary as requested by the Examiner. Applicant has also filled in the serial numbers of the co-pending applications on page 1 as requested by the Examiner. Applicant has also amended the title as requested by the Examiner.

The specification has also been amended to insert the patent numbers of issued U.S. patents incorporated by reference in the specification.

In the Claims

Rejection Under 35 USC 102(b)

The Examiner rejected claims 1-7, 11, 13-15, 17-19, 21-30, and 34-42 under 35 U.S.C. § 102(b), as being anticipated over *Shiell, et al.*, U.S. Patent No. 5,850,543 (hereinafter *Shiell*). Applicant respectfully traverses the rejection of claims 1, 3-18, and 34-38.

Claims 1, 3-18

With respect to claim 1, Applicant has amended claim 1 to incorporate the limitations of now canceled claims 2 and 12. The Examiner rejected claim 12 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell et al.*, U.S. Patent No. 5,850,543 (hereinafter *Shiell*). With respect to claim 12, the Examiner acknowledged the prior art does not expressly show a branch target address cache configured to store a length of a branch instruction presumed present in a cache line. However, the Examiner asserted the speculative branch information associated with a previously executed branch instruction comprising a length of the branch instruction presumed present in the cache line is nonfunctional descriptive material, citing *In re Lowry*. Applicant respectfully asserts that the branch instruction length information is not nonfunctional descriptive material. Applicant's specification clearly describes functions of the branch instruction length information, an embodiment of which is shown and described by the LEN field 448 stored in each BTAC entry. For example, the LEN field is used to calculate a call instruction return address for storage in a speculative call/return stack. For another example, the LEN field is used to determine whether a speculative BTAC prediction is erroneous by comparing the branch instruction length provided by the BTAC with a decoded length of the instruction. Consequently, the branch instruction length information enables the BTAC to provide improved branch prediction while accomplishing correct program execution. Therefore, Applicant respectfully asserts the branch instruction length information is not nonfunctional descriptive material, and the Examiner is not at liberty to ignore the recited limitation. Just as the Federal Circuit stated with respect to Lowry's data structures, the branch instruction length information stored in the branch target address cache are "more than a mere abstraction," they are "specific electrical or magnetic structural elements in a memory." They are "physical entities that provide increased efficiency in computer operation." Therefore, Applicant respectfully asserts that *Shiell* does not anticipate or obviate amended claim 1.

Applicant respectfully asserts *Shiell* does not anticipate or obviate dependent claims 3-11 or 13-18 because they depend from independent claim 1, which is not anticipated or obviated by *Shiell* for the reasons discussed above.

Claims 34-38

With respect to claim 34, Applicant has amended claim 34 to incorporate the limitation regarding the caching of indications of whether each of the previously executed branch instructions spans an instruction cache line of claim 16. The Examiner rejected claim 16 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell et al.*, U.S. Patent No. 5,850,543 (hereinafter *Shiell*). With respect to claim 16, the Examiner acknowledged the prior art does not expressly show a branch target address cache configured to store an indication of whether a branch instruction presumed present in a cache line spans more than one line in the instruction cache. However, the Examiner asserted the speculative branch information associated with a previously executed branch instruction comprising an indication of whether a branch instruction presumed present in a cache line spans more than one line in the instruction cache is nonfunctional descriptive material, citing *In re Lowry*. Applicant respectfully asserts the indication of whether the branch instruction presumed present in the cache line spans more than one line in the instruction cache may alter how the microprocessor operates by affecting which cache line will be fetched next if the branch instruction is predicted taken. In particular, if the branch instruction spans more than one cache line, then the next sequential cache line must necessarily be fetched before the cache line at the target address may be fetched so that all the bytes of the branch instruction can be issued to the pipeline for execution; however, if the branch instruction does not span more than one cache line, then the cache line at the branch target address may be fetched. Consequently, the indication of whether the branch instruction spans more than one cache line enables the BTAC to provide improved branch prediction while accomplishing correct program execution. Therefore, Applicant respectfully asserts the indication of whether the branch instruction spans more than one cache line is not nonfunctional descriptive material, and the Examiner is not at liberty to ignore the recited limitation. Just as the Federal Circuit stated with respect to Lowry's data structures, the indications of whether the branch instruction spans more than one cache line stored in the branch target address cache are "more than a mere abstraction," they are "specific electrical or magnetic structural elements in a memory." They are "physical entities that provide increased efficiency in computer operation." Therefore, Applicant respectfully asserts that *Shiell* does not anticipate or obviate amended claim 34.

Applicant respectfully asserts *Shiell* does not anticipate or obviate dependent claims 35-38 because they depend from independent claim 34, which is not anticipated or obviated by *Shiell* for the reasons discussed above.

Rejection Under 35 USC 103

The Examiner rejected claims 31-33 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell* and *Dietz et al.*, U.S. Patent No. 5,634,103 (hereinafter *Dietz*). Applicant respectfully traverses the Examiner's rejections.

Broadly speaking, *Dietz* teaches a microprocessor that fetches a group or set of instructions from an instruction cache. The set of instructions may include a branch instruction. The instructions following the branch instruction in the set are referred to by *Dietz* as instructions in the sequential execution path. A prediction is made of whether the branch instruction will be taken or not taken. If the branch instruction is predicted taken, prior art processors flush the instructions in the sequential execution path. However, *Dietz* teaches speculatively dispatching for execution the instructions in the sequential execution path if the execution units of the microprocessor are idle, even though the branch instruction is predicted taken, thereby making the instructions in the sequential execution path to be in a speculative execution path. The advantage of *Dietz*'s method is that if the prediction was incorrect – i.e., the branch was not taken – the instructions in the sequential execution path will already have been dispatched for execution. When the instructions in the sequential execution path are speculatively dispatched, i.e., when they are placed into the speculative execution path, their associated speculative bit is set. If the branch instruction is later determined to have been correctly predicted taken, any instruction with a set speculative bit has its valid bit cleared, thereby effecting a flush of the instruction. Thus, Applicant notes that *Dietz*'s speculative bit may be set for non-branch instructions in the speculative instruction path.

Claims 31-33, 43-49

With respect to claim 31, the Examiner asserts that *Dietz* teaches a processor in which each instruction has a corresponding speculative bit indicating whether the instruction is within the speculative execution path. If the speculative path is resolved as incorrect,

instructions tagged as speculative are flushed. Applicant respectfully asserts that *Dietz* does not teach an indicator associated with an instruction in an instruction buffer indicating whether the instruction associated with the indicator is a previously executed branch instruction whose target address provided by a branch target address cache has been speculatively branched to by the microprocessor, as recited in amended claim 31. First, *Dietz*'s speculative bit does not indicate whether an instruction associated therewith is a previously executed branch instruction whose target address provided by a branch target address cache has been speculatively branched to by the microprocessor, as recited in amended claim 31. Rather, *Dietz*'s speculative bit indicates whether an instruction, regardless of whether it is a branch or a non-branch instruction, is in a speculative execution path by virtue of a previously predicted taken branch instruction, not that the instruction is a branch instruction that was speculatively predicted taken.

Furthermore, *Dietz* teaches that it is instructions in the execution pipeline of his processor (i.e., elements 22, 28, and 30; see col. 3, lines 62-65), which are below the dispatch unit (element 20 of Fig. 1) in the pipeline, that have a speculative bit. This is because until the dispatch unit dispatches the instruction, it cannot be known whether the instruction is in a speculative execution path (see block 66 of Fig. 2). This further implies that instructions in *Dietz*'s instruction queue (element 19 of Fig. 1) cannot have a speculative bit since the instruction queue precedes the instruction dispatch unit, i.e., when the instructions are in the instruction queue it cannot be known yet whether the instructions are in a speculative execution path. Therefore, it would not have been obvious to modify *Shiell*'s instruction buffer to add *Dietz*'s speculative bits thereto since *Shiell*'s instruction buffer (element 60 of Fig. 2, which is included in fetch unit 26 of Fig. 1) also precedes *Shiell*'s instruction scheduler (element 36 of Fig. 1). For each of the reasons stated above, Applicant respectfully asserts that *Shiell* and *Dietz* do not obviate claim 31.

Applicant respectfully asserts *Shiell* and *Dietz* do not obviate dependent claims 32-33 and 43-49 because they depend from independent claim 31, which is not obviated by *Shiell* and *Dietz* for the reasons discussed above.

Claims 50-65

Claim 50 is a new claim which includes the combined limitations of the original claims 1, 2 and 16. For the reasons stated above with respect to amended claim 34 (which has been amended to incorporate the limitations of claim 16), Applicant respectfully asserts that *Shiell* does not anticipate or obviate new claim 50.

Applicant respectfully asserts *Shiell* does not anticipate or obviate dependent claims 51-65 because they depend from independent claim 50, which is not anticipated or obviated by *Shiell* for the reasons discussed above.

Claims 66-70

Claim 66 is a new claim which includes the combined limitations of claims 34 and 12. For the reasons stated above with respect to amended claim 1 (which has been amended to incorporate the limitation of caching a length of each of previously executed branch instruction in a branch target address cache of claim 12), Applicant respectfully asserts that *Shiell* does not anticipate or obviate new claim 66.

Applicant respectfully asserts *Shiell* does not anticipate or obviate dependent claims 67-70 because they depend from independent claim 66, which is not anticipated or obviated by *Shiell* for the reasons discussed above.

The Examiner has indicated additional prior art which is made of record and not relied upon. None of these references anticipate or obviate applicant's invention.

For all of the reasons advanced above, Applicant respectfully submits that claims 1, 3-11, 13-18, 31-38, and 43-70 are in condition for allowance. Reconsideration of the rejections is requested, and Allowance of the claims is solicited.

Applicant earnestly requests the Examiner to telephone him at the direct dial number printed below if the Examiner has any questions or suggestions concerning the application or allowance of any claims thereof.

Respectfully submitted,

James W. Huffman
Huffman Law Group, P.C.
Registration No. 35,549
Customer No. 23669
1832 N. Cascade Ave.
Colorado Springs, CO 80907
719.475.7103
719.623.0141 fax
jim@huffmanlaw.net

Date: 6-7-04

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By: Vicki J. Hoy